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Digital Control of Variable Frequency Interleaved DC-DC Converter

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***Abstract* – This paper represents a design and implementation of a digital control of variable frequency interleaved DC-DC converter using a digital signal processor (DSP). The digital PWM generation, current and voltage sensing, user interface and the new period and pulse width value calculation with DSP STM32F407VGT6 are considered.**

Typically, the multiphase interleaved DC - DC converters require a current control loop in each phase to avoid imbalanced current between phases. This increases system costs and control complexity. In this paper the converter which operates in discontinuous conduction mode is designed in order to reduce costs and remove the current control loop in each phase. High current ripples associated with this mode operation are then alleviated by interleaving.

Pulse width modulation (PWM) is one of the most conventional modulation techniques for switching DC - DC converters. It compares the error signal with the sawtooth wave to generate the control pulse. This paper shows how six PWM signals phase-shifted by 60 degrees can be generated from calculated values.

To ensure that the measured values do not contain disturbances and in order to improve the system stability the digital signal is filtered. The analog to digital converter's (ADC) sampling time must not coincide with the power transistor's switching time, therefore the sampling time must be calculated correctly as well.

Digital control of the DC-DC converter makes it easy and quickly to configure. It is possible for this device to communicate with other devices in a simple way, to realize data input by using buttons and keyboard, and to display information on LED, LCD displays, etc.

***Keywords* – switching converter, digital control, pulse width modulation, digital signal processors.**

I INTRODUCTION

A switching converter transforms an one voltage level into another for a given load by switching action of semiconductor devices. In the past, most of power electronic converters employed analog control methods. The reason is that digital controllers of the previous era had bandwidth problems. In the recent years the situation has changed significantly. The speed and functionality performance of the DSPs has improved. They are also available at a much lower cost. The advantage of the digital controller is that it is programmable and offers more functionality to the system compared to the analog controllers. Novel control algorithms and methods with DSP can be realized.

Interleaving control schemes are widely used in converter applications [1, 3, 5]. Merits of such control methods are reduction of input/output current or voltage ripples and volume, and increase in the processed power capacity of converters. In discontinuous conduction mode (DCM) the reverse-recovery losses of the boost diode are eliminated and switching losses can be reduced. Current in choke only depends on the on-time of transistor but does not depend on the current in the previous periods. This allows to improve dynamic and stability of converter even without current sensors in each phase.

Compared to DCM with constant switching frequency variable frequency mode yields lower total harmonic distortion (THD) of the input current and smaller peak inductor currents and results in lower switching and conduction losses. It is easier to achieve interleaving control of converters with constant frequency of operation [2, 4, 6, 8]. It is more difficult to realize interleaving features of a converter with variable frequency operation. This will be the focus of the article.

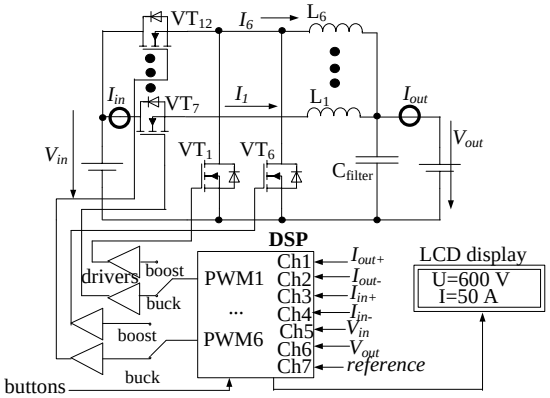

Fig. 1. DSP controlled DC-DC converter structure

Figure 1 shows the structure of DC-DC converter. It has six phases and is bi-directional as it can work in both buck and boost mode. If boost mode is selected, transistors VT1...VT6 are being switched on and off but VT7...VT12 remain turned off and vice versa. In order to calculate new period and pulse length values seven analog values are measured and converted into digital signals. Buttons and LCD display provide user interface. At present it is used to charge and discharge accumulator or ultracapacitor with maximal power 10 kW. Soft start must be realized in order to feed a resistive load or an electric drive.

Using the inductance as well as the input and output voltage the required on-time and off-time are

calculated to ensure operation in boundary conduction mode (BCM). It is shown in figure 2. The required phase shift value is determined by using the calculated switching period to guarantee optimal ripple cancelation. The current tracking can be done via open-loop control and no current sensing is necessary.

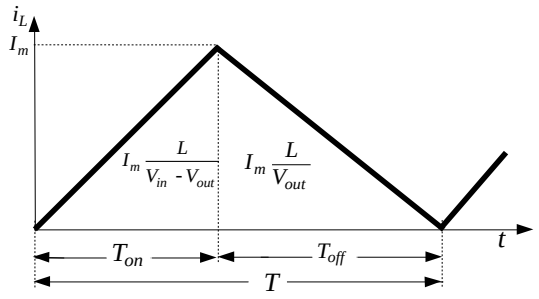

Fig. 2. Inductor current at boundary conduction mode

In BCM the peak current in choke is twice the average current [5]. The summary output current I_{out} of n phase converter is sum of all choke currents. Peak current in choke can be expressed as shown below.

$$I_m = \frac{2 \cdot I_{out}}{n} \quad (1)$$

I_m can be used not only to maintain the desirable output current but also to control input current and output voltage. It can be done if I_m is output of proportional-integral (PI) regulator that is shown in figure 3.

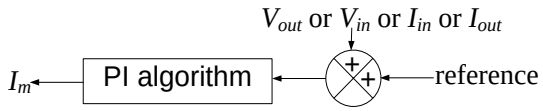

Fig. 3. Calculation of I_m by PI regulator

An error in the voltage measurement could cause a drop out of the BCM. In such a case entering into continuous conduction mode (CCM) has to be avoided to prevent overcurrent. Therefore it is beneficial to move slightly into DCM. Inductance is multiplied by the coefficient to get the a little enlarged DCM switching period and to stay into DCM.

II MATERIALS AND METHODS

In order to control the DC-DC converter the STM32F407VGT6 microcontroller (MCU) is used. This ARM Cortex-M4 32 bit MCU with floating-point unit has 210 DMIPS, up to 1MB Flash, 194 KB RAM, 17 timers (including the general purpose ones), 3 analog to digital converters (ADC), 15 communication interfaces. MCU maximal operating frequency is 168 MHz. It also includes a full set of digital signal processor (DSP) instructions and a memory protection unit (MPU).

The program code was written in C language and IAR Embedded Workbench for ARM integrated development environment (IDE) was used. The IAR Embedded Workbench for ARM is a window-based software development platform that combines a robust and modern editor with a project manager. It integrates all the tools needed to develop embedded applications including a C/C++ compiler, a macro assembler, a linker/locator and a HEX file generator. The IAR Embedded Workbench helps to expedite the development process of embedded applications by providing the IDE with project management tools and editor, highly optimizing C and C++ compiler for ARM, automatic checking of C rules, CMSIS (Cortex Microcontroller Software Interface Standard) compliance, linker and librarian tools, JTAG support.

To measure signals the Tektronix TPS 2024 digital oscilloscope was used. The oscilloscope has 200 MHz bandwidth and 2 GS/s real time sample rate. The TPS2024 input connector shells are isolated from each other and from earth ground.

The general-purpose timers (that are a part of a MCU) consist of a 16-bit auto-reload counter driven by a programmable prescaler. They may be used for a variety of purposes, including measuring the pulse lengths of input signals (input capture) and generating output waveforms (output compare and PWM). Pulse lengths and waveform periods can be modulated from a few microseconds to several milliseconds. The timers are completely independent and do not share any resources. They can be synchronized together.

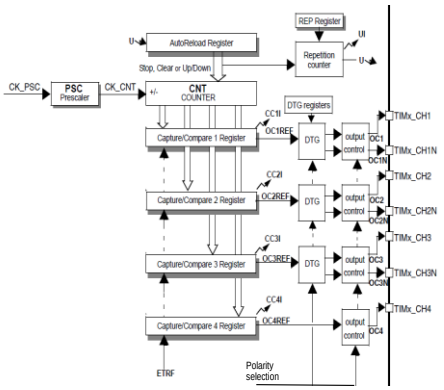

Fig. 4. Fragment of timer's block diagram [7]

Figure 4 shows PWM generation part of timer's block diagram. Each timer has four capture/compare registers. The counter and the auto-reload register can be written and read by software. The content of the preload register is transferred into the shadow register permanently or at each update event. The update event is generated when the counter reaches an overflow. It can also be generated by a software. PWM signal frequency is determined by the value of the auto-reload register and a pulse length is determined by the value of capture/compare register in timer's PWM mode.

A 12-bit ADC has up to 19 multiplexed channels allowing it to measure signals from 16 external sources. The analog to digital conversion of the channels can be performed in single, continuous, scan or discontinuous mode. The main features of ADC are

interrupt generation at the end of conversation and dual and triple mode with configurable direct memory access (DMA) to data storage.

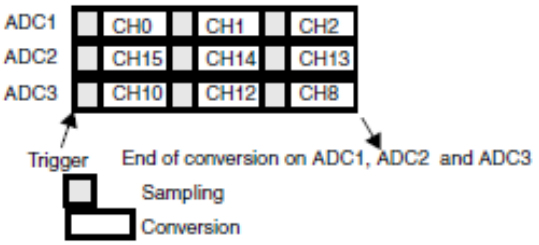

Fig. 5. Triple ADC mode of 9 channels

To provide control, protection and user interface of DC-DC converter it is necessary to measure 7 analog signals. In this case ADC's triple mode (Fig. 5) was selected to provide conversation of these signals as fast as possible. Maximal frequency of ADC clock is 36 MHz. Three ADC's clock cycles are required for signal sampling and 12 for conversation. The time required for analog to digital conversation can be calculated:

$$t_{ADC} = \frac{N_{cycle}}{f_{CLOCK_{ADC}}} = \frac{15}{36 \cdot 10^6} = 417ns \qquad (2)$$

At the end of conversation three DMA transfer requests are generated. Then, the three transfers from the ADC register to SRAM take place: first, the ADC1 converted data, then the ADC2 converted data and finally the ADC3 converted data. This process is repeated for each three new conversations to avoid loss of the data already stored in the ADC register.

III Results and Discussion

A. ADC starting time

The Interrupt Service Routine (ISR) of a timer is the heart of the control software. The ISR has the highest priority of execution. During the interrupt of overflow of the timer's counter (IRQ1) the new period and pulse length values are set for each of six timers. In the capture/compare ISR of the timer (IRQ2) ADC is started and the new period and pulse length values are calculated.

Two major sources of electromagnetic interference (EMI) in DC-DC converter are dv/dt and di/dt during the switching times of the power transistors. EMI affects the accuracy of ADC. Therefore, it is important to measure current and voltage at a moment switching of transistors does not take place. Switching off the transistors interrupts current for a short time and produces significant EMI.

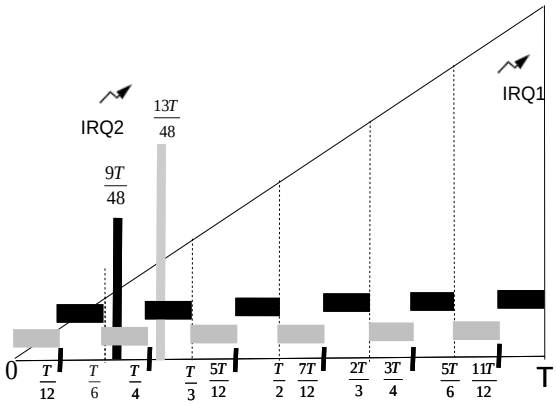

Fig . 6. Selection of ADC's starting time

The transistors are controlled by microcontroller and it is possible to calculate the starting time of closing of the transistors. The transistor has the same pulse length in each phase. The pulses are only shifted in phase by 60 degrees or by sixth of the period (T). Figure 6 shows how to choose ADC conversion time without transistor switching off. The period is divided into 12 parts and it is determined in which part first channel's transistor switching off moment is. Switching moments of the transistors in other channels are in the other areas of the figure in the same color. So ADC conversion can be made in any area of a different color. To leave more time for calculation the ADC starting time is chosen in the beginning of period - 9T/48 in one case and 13T/48 in the other.

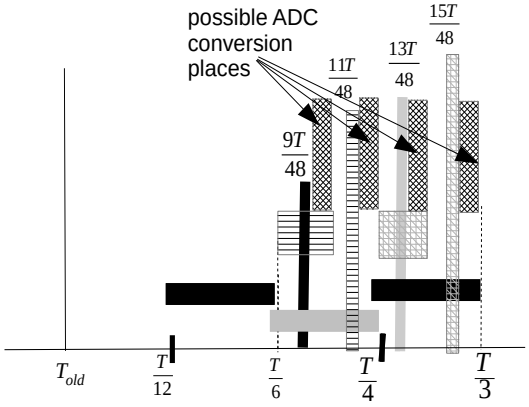

Fig. 7. Selection of ADC conversation time

The transistor is controlled by PWM and the pulse length is determined by the timer's value stored in the capture/compare second register. This value is calculated in the IRQ2 program, which can be extended in order to find the position of value of the pulse length (CCR) and calculate new ADC starting time (p):

```
[1] if (CCR<=(T/6))
[2]    {   if (CCR<=(T/12))
[3]         p=9T/48;         //ADC starting
    time 1
[4]        else
[5]         p=13T/48;}                  //ADC
    starting time 2
[6] else if (((T/6)<CCR)&&(CCR<=(T/3)))
[7]    {   if (CCR<=(T/4))
[8]               p=9T/48;
[9]            else
[10]                 p=13T/48;}
[11]
       ..............
```

The PWM signals from the previous period with length more than T/6 can also cause EMI. If the sum of the pulse time and the phase shift time exceeds T/6, then the phase with switch-off time of the transistor closest to the above calculated ADC starting time can be calculated with number up rounding to the nearest whole number as in (4). And then the switch-off time of the transistor of this phase can be calculated by using (5).

$$t_{pulse\_old} + n \cdot \frac{T_{old}}{6} \geq \frac{T}{6} \tag{3}$$

$$n \geq\approx \frac{6 \cdot (\frac{T}{6} - t_{pulse\_old})}{T_{old}} \tag{4}$$

$$p_1 = t_{pulse\_old} + n \cdot \frac{T_{old}}{6} \tag{5}$$

The program addition checks whether the switch-off time of transistor does not match the previously calculated ADC conversation time. If it does, a different ADC starting time is selected. Figure 7 shows the final algorithm of selection of the ADC starting time.

```
[12]    if((p1>=(T/6))&&(p1<(5*T/48))&&(p==(9*
    T/48))
[13]       {   p=11T/48; }          //ADC
    starting time 1a
[14]    else if
    ((p1>=(14*T/6))&&(p1<(T/4))&&(p==(13*T/48)
    )
[15]       {   p=15*T/68;}          //ADC
    starting time 2a
```

The previously calculated time required to perform ADC conversion is 417ns. The maximum time without EMI is T/48. It means that the minimum period of timer must be 20 μs or maximum frequency of impulse in each phase must be 50 kHz.

Figure 8 shows oscillogram of first channel PWM signal and one DSP output pin that is set when IRQ2 starts and that is reset when IRQ2 ends. It shows how much time is necessary for calculation of I_m, new period, pulse-time and new ADC starting time and so on. This time is less than the critical one.

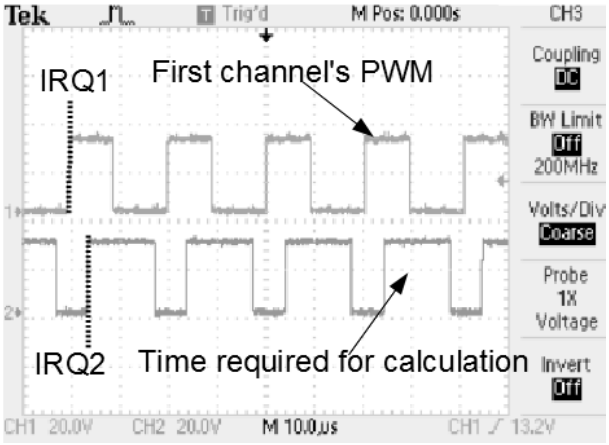

Fig. 8. Oscillogram of ADC's starting time

B. Digital filtering

The period value is calculated by using the (6) were I_m is feedback error calculated by using the proportional-integral (PI) algorithm, L is the inductance of choke, V_{in} is the input voltage and V_{out} is the output voltage. The equation shows that a small measurement error or noise induced error in sampled V_{out} value causes big error in period value.

$$T = I_m L \frac{V_{in}}{(V_{in} - V_{out}) \cdot V_{out}} \tag{6}$$

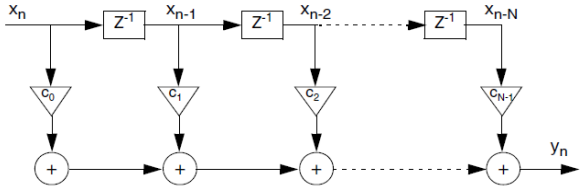

Fig. 9. Block diagram of FIR filter

In order to improve the stability of the converter the finite response filter (FIR) for V_{out} was used. The figure 9 shows the block diagram of the FIR filter: x_n is the input signal, y_n is the output signal, c_i are the filter coefficients, also known as tap weights and N is the filter order. An N th-order filter has N+1 terms on the right-hand side. The output value of filter is calculated by using (7).

$$y[n] = \left(c_0 x[i] + c_1 x\left[i-1\right] + c_N x[i-N]\right)$$

$$V_{out} = \left(\frac{1}{4}V_{outi} + \frac{1}{4}V_{out(i-1)} + \frac{1}{4}V_{out(i-2)} + \frac{1}{8}V_{out(i-3)} + \frac{1}{8}V_{out(i-4)}\right) \tag{7}$$

Four previously measured V_{out} values are stored in memory and when current ADC value is read, the filtered V_{out} value is calculated by (7). The filter coefficients are set equal to $1/2^n$ because shifting is faster then dividing. Older values have less influence on the filtered value if the coefficients are smaller. After calculation all the historical values are overwritten, the newest value is stored in memory and

the oldest value is erased. The circular buffer is shown in a fragment of the program.

```
[16]            Vout4=Vout3;
[17]            Vout3=Vout2;
[18]            Vout2=Vout1;
[19]            Vout1=Vout0;
        Vout0=ADCTripleConvertedValue[5];
```

The ripple of output voltage is not large but ADC's starting time varies as discussed above and it can lead to measurement error. The digital filtering of voltage value reduces this error and eliminates it's influence on stability of the interleaved converter.

C. Phase-shifted impulses generating

Six gate signals are needed to control the six-phase DC-DC converter. The phase shift between phases of converter in N-phase converter system can be calculated as in (8).

$$\varphi = \frac{360°}{N} = \frac{360°}{6} = 60° \tag{8}$$

The power transistors are controlled by PWM signal of microcontroller. Frequency and pulse length are calculated in each period. In overload ISR of the counter of the first channel's timer the new period and pulse width values of all timers are recorded in corresponding register but they are updated when an update event occurs. This event is generated when counter overload of corresponding timer occurs.

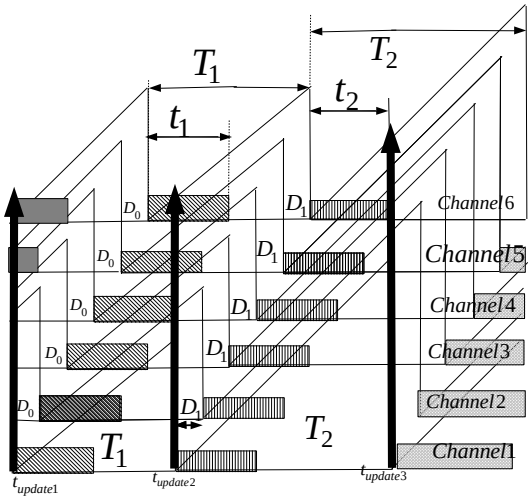

Fig. 10. PWM signals

As interleaved DC-DC converter has 6 phases, PWM pulses must be shifted by 60 electrical degrees. As can be seen in figure 10 the phase shift (D_0=D_1) does not change together with frequency, which is not correct. This problem can be solved.

Rapid decrease of the period causes duplication of PWM pulses and consequently the malfunction of the DC-DC converter. The maximum speed of decrease in period for the pulses not to overlap is one sixth of the value of the previous period if the pulse width is less than 5/6 of the period as shown in figure 11. The converter does not have a current sensor in each phase. So it is necessary to increase a period a little in order not to get into uncontrollable continuous conduction mode. So the pulse length never exceeds 5/6 of the period.

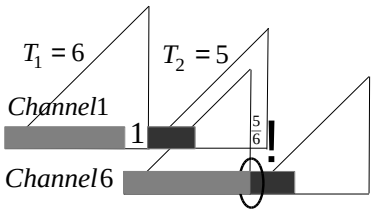

Fig. 11. Determination of maximum speed of period change

50 kHz was chosen as the minimum switching frequency. The maximum value of a period is set to be equal to 1 ms so the frequency is 1 kHz. Further increase in the period creates very short PWM signals that produce big noise. It is possible to calculate the number of periods (n) in order to change the frequency from the lowest one to the highest one. It follows from (9) and (10) that 21 period is necessary to reach the minimum frequency. Such a time allows to respond to the load change.

$$\left(\frac{5}{6}\right)^n = \frac{f_{lowest}}{f_{highest}} = \frac{1}{50} = 0,02 \tag{9}$$

$$n = \log_{\frac{5}{6}} 0,02 \approx 21 \tag{10}$$

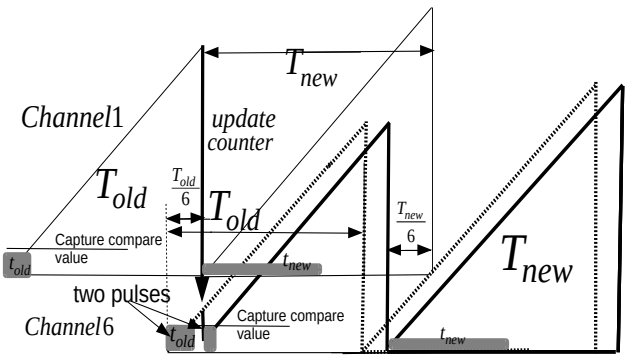

Fig. 12. Realization of phase shift with counter update

Phase shift can be done by setting a counter value when the IRQ1 occurs. This counter value is calculated so that timer's period of the corresponding channel ends at point that provides right phase shift of new pulses. Figure 12 shows the implementation of the phase shift with a counter update. As can be seen in the figure the counter value can be calculated from the isosceles triangles by (11) where n is the number of channel from 2 to 6 can be written. The disadvantage of this method is that an extraneous pulse can be generated when changing the counter's value.

$$CNT = \frac{(n-7)\cdot T_{old}}{6} + \frac{(n-1)\cdot (T_{old} - T_{new})}{6} \tag{11}$$

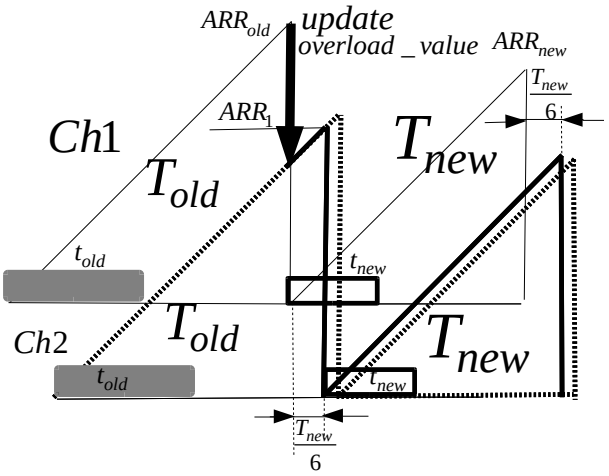

Fig. 13. Realization of phase shift with overload value update

The phase shift can be implemented by updating the overload value of the timer which is value of the auto-reload register (ARR). In this case the period value is either prolonged or shortened. As discussed above the increase in period can not exceed 1/6 of it's length. This means that changing the period by updating it only affects the last sixth of the period where there is no impulse. As demonstrated in figure 13 the new value of ARR is set in the IRQ1. This value is selected so that it ensures the overload of the n-channel's timer in time that corresponds to required phase shift. The ARR value that must be set to provide a correct phase shift can be easily calculated by using the (12).

$$ARR_1 = ARR_{old} - \frac{(n-1)\cdot ARR_{old}}{6} + \frac{(n-1)\cdot ARR_{new}}{6} \quad (12)$$

D. Hardware implementation

The figure 14 shows hardware implementation of DSP controlled 6 phase interleaved DC-DC converter. It is possible to realize communication with a device via USB, CAN, I2C, UART, SPI, touch screen, digital microphone, etc. LCD display (1), LEDs (5) and buttons are selected in this case as cheapest solution. The power transistors (4) are placed on the radiator plate. DSP board (3) is connected via the cable (2) to the buttons.

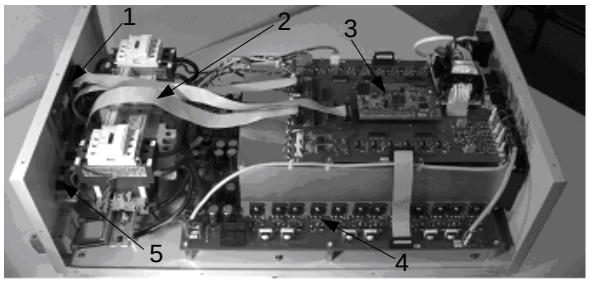

Fig. 14. Hardware of interleaved DC-DC converter

IV CONCLUSION

It is possible to design interleaved DC-DC converter without measuring current in each phase. So it is necessary to implement digital control to implement the open-loop control.

In order to ensure that the measured values do not contain disturbances and to improve the system stability the simple FIR digital filter is implemented.

The analog to digital converter's starting time must not coincide with the power transistor's switching time, therefore the ADC starting time calculation and algorithm is used.

Six gate signals are needed to control the six-phase DC-DC converter. This paper describes the algorithm for phase shifting of signals from calculated values. This algorithm was implemented with some limitations and requires future investigations.

Digital control of the DC-DC converter makes it easy and quickly to configure. Such implementation of the hardware of the converter needs a smaller number of components and is less costly. The input of data is realized simply by using buttons and potentiometer, while output of data - by using LEDs and the LCD display.

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